

ABSTRACT

A memory circuit (14) having features specifically adapted to permit the memory circuit (14) to serve as a video frame memory is disclosed. The memory circuit (14) contains a dynamic random access memory array (24) with buffers (18, 20) on input and output data ports (22) thereof to permit asynchronous read, write and refresh accesses to the memory array (24). The memory circuit (14) is accessed both serially and randomly. An address generator (28) contains an address buffer register (36) which stores a random access address and an address sequencer (40) which provides a stream of addresses to the memory array (24). An initial address for the stream of addresses is the random access address stored in the address buffer register (36).